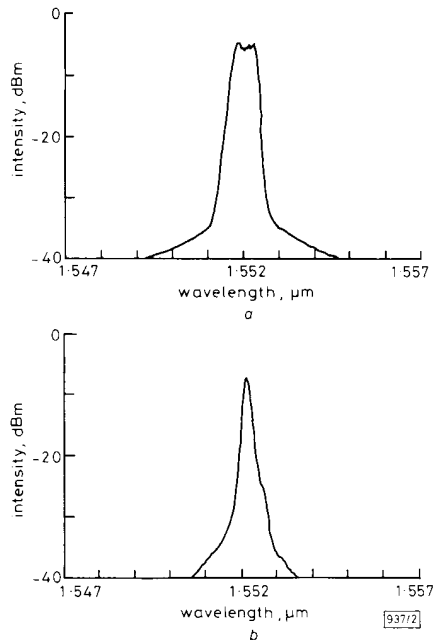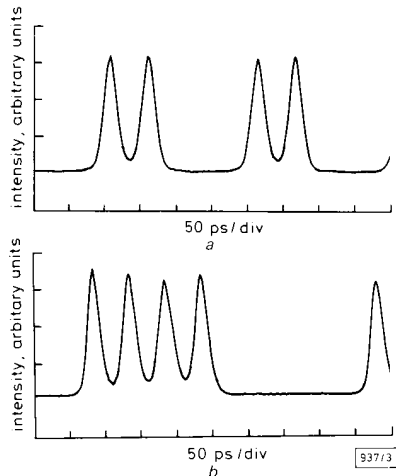ters. This system is stable since the cascaded EDFAs can automatically control the soliton power level. Although strong interaction may occur after propagation over more than

Fig. 2 *Output spectra of the MQW DFB LD when gain switching technique is applied*

a Without FPR
b With FPR

Fig. 3 *Coded soliton pulse waveforms at 20 Gbit/s transmitted over 200 km*

a Coded solitons as ⟨0011001100⟩
b Coded solitons as ⟨0111100001⟩
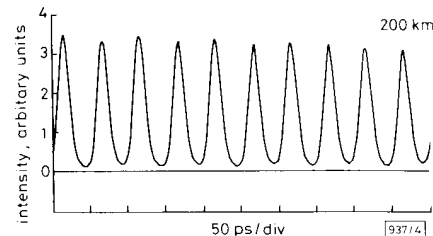
Fig. 4 *20 GHz soliton transmission over 200 km*

500 km, it can be said that soliton communication has great potential for realising ultrahigh bit-rate optical communication systems.

In summary, we have shown that it is possible to send a 20 Gbit/s soliton signal over 200 km using erbium-doped fibre amplifiers. This means that EDFAs are very promising as soliton amplifiers.

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HIGH-PERFORMANCE ALGORITHMIC SWITCHED-CURRENT MEMORY CELL
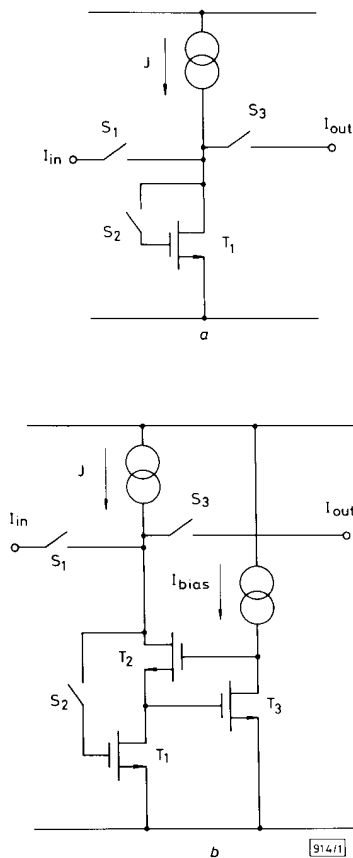
Indexing terms: Memories, Current mode

A new high-performance algorithmic switched-current memory cell with greatly improved charge injection performance is described. The new cell uses algorithmic means to achieve an improvement in charge injection of two orders of magnitude and does not rely on matching.

Introduction: There is tremendous interest in the application of switched-current (SI) techniques to the design of analogue filters and data convertors. SI techniques offer major advantages over conventional switched-capacitor techniques in the

current commercial environment, where process technology is driven by the needs of digital circuitry. SI techniques are able to function with reduced supply voltages, because of their current domain operation, and do not require special process options (such as double-poly), since a high quality linear capacitor is not required. SI circuits are thus able to cohabit modern scaled digital ICs with digital logic, enabling economic single chip solutions to be realised for the many system applications that require an analogue interface.

The switched-current (SI) memory cell, also known as the current copier, was initially conceived[1-4] to overcome the inherent matching limitations of continuous time current mirrors. Initially, the cell found application in high performance D/A convertors[2] and more recently as a delay element for the realisation of analogue filters.[5] Many new applications are currently under investigation.[6] In this letter we propose a new high performance algorithmic SI memory cell incorporating a novel switching arrangement to enhance current transfer accuracy.

Existing memory cells: The basic switched-current memory cell[1] is illustrated in Fig. 1a. At ϕ_1, switches S_1 and S_2 are closed, S_3 open. T_1 is thus diode-connected, and a drain-source current of $J + I_{in}$ will charge its gate-source capacitance, C_{gs}. The V_{gs} established is that required to maintain the current $J + I_{in}$ when the input is removed, thus memorising the input. At ϕ_2, S_1 and S_2 are open, S_3 closed. Since T_1 maintains a drain current of $J + I_{in}$ the output current is $-I_{in}$ which is an inverted direct copy of the input. Note that the output of the cell is a discontinuous copy of the input. For 'continuous' operation two basic cells may be cross-coupled to form a dynamic mirror.[4]
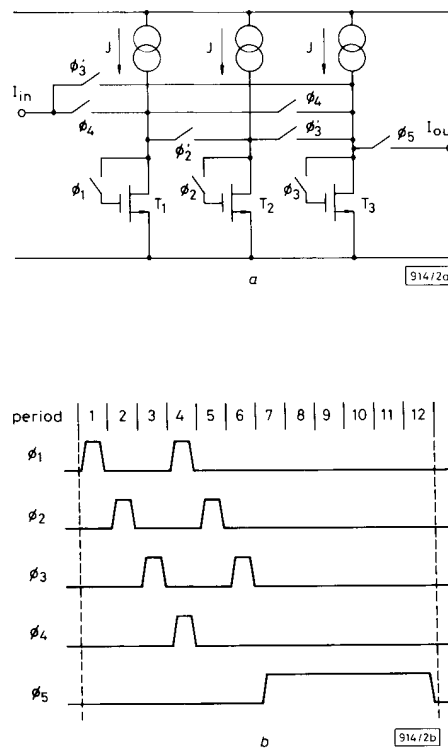
There are two primary problems with this basic SI cell. The channel length modulation effect causes an error in the output, if the V_{DS} of T_1 is not the same in the sampling and retrieval phases. The second is that when S_1 and S_2 open, a proportion of their channel charge is dumped onto the C_{gs} of T_1, causing a ΔV_{gs} and hence an output current error. The charge injection from S_1 can be eliminated by ensuring that S_2 opens slightly before S_1; which can be achieved by delaying the falling edge of S_1's clock.

There are several techniques for tackling the channel length modulation problem,[7,8] of which the use of a cascoded or a regulated cascode transconductor[8] appears the most promising. A SI memory cell based on the regulated cascode is shown in Fig. 1b. It has been shown that, by operating the storage transistor of the regulated cascode in its saturated region, an improvement of three orders of magnitude is possible in the output resistance of the cell. An improvement of two orders of magnitude is still possible with unsaturated operation, which gives a reduced g_m, which is constant with I_{DS}, an advantage from the charge injection viewpoint.

With the vast improvement in output resistance possible using cascoding, charge injection has become the dominant performance limitation. There are a number of techniques for reducing the effects of charge injection.[7] The most common rely on various matching mechanisms to achieve charge injection cancellation, such as the use of dummy switches. We propose an algorithmic memory cell which achieves cancellation without the need for matching, resulting in a significant performance improvement.

Algorithmic memory cell: Fig. 2a shows the proposed algorithmic memory cell, which uses five phases and three basic memory cells. The required clocking scheme is illustrated in Fig. 2b; it should be noted that phases ϕ_2' and ϕ_3' (not shown) are the same as ϕ_2 and ϕ_3 with a delayed trailing edge to avoid additional charge injection.

a

b

Fig. 1 *Basic current memory cell*

  a Single transistor memory
  b Regulated cascode memory

a

b

Fig. 2 *Algorithmic memory cell*

  a Structure
  b Timing diagram

The concept of the circuit is to access the charge injection error of a memory cell, invert it and then pass it through the same cell again. The algorithmic nature of this process ensures that the charge injection error is cancelled without the need for matching.

In periods 1 and 2 the charge injection error of the first two cells is accumulated. In period 3 the charge injection error of the third cell is added. This is done in the presence of the input current, I_{in}, to ensure that the g_m of T_3 is the same as it will be in the output phase, ϕ_5. In period 4 the output of the third cell is summed with the input, I_{in}, leaving just the accumulated charge injection errors to be sampled by the first cell. The uneven number of signal inversions around the loop ensures that the charge injection error of the first cell in period 1 cancels with its charge injection in period 4. The same cancellation occurs in the second cell and then again in the third cell, where the input signal is reintroduced. Finally, during periods 7–12, the input current, I_{in}, is output together with any residual error. Thus using the proposed cell, charge injection errors have been cancelled, according to the following relationship:

$$I_{out} = -I_{in} - (\delta_{14} - \delta_{11}) + (\delta_{25} - \delta_{22}) - (\delta_{36} - \delta_{33}) \quad (1)$$

where δ_{ij} is the charge injection in the ith cell during period j.

Simulated results: The performance of the proposed cell was simulated using HSPICE and the parameter set of a typical $2\,\mu m$ N-well CMOS process. All the switches used were $2/2\,\mu m$ (W/L); the memory transistors were $60/20\,\mu m$ in the basic cell, $100/20\,\mu m$ in the saturated regulated cascode and $25/20\,\mu m$ in the basic cell, $100/20\,\mu m$ in the saturated regulated cascode and $25/20\,\mu m$ in the unsaturated regulated cascode. The bias current, J, used in all cases was $100\,\mu A$ and the width of each clock pulse was 400 ns.

The improvement in charge injection error offered by the proposed algorithmic memory cell is illustrated in Fig. 3,
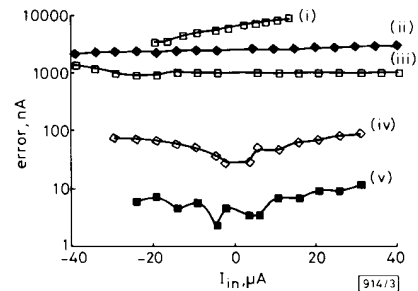

Fig. 3 *Charge injection performance*
(i) Basic cell with single transistor
(ii) Basic cell with saturated regulated cascode
(iii) Basic cell with unsaturated regulated cascode
(iv) Algorithmic cell with saturated regulated cascode
(v) Algorithmic cell with unsaturated regulated cascode

where its performance is compared with that of the basic cell, using a single transistor (Fig. 1a) and a regulated cascode (Fig. 1b), with its memory transistor in saturated and unsaturated operation. To give a strict comparison the performance of the basic cell is compared with that of the algorithmic cell (Fig. 2a) with its basic transistors also replaced by regulated cascodes, so that the main source of error is charge injection. It can be seen that the proposed cell offers a significant improvement of about two orders of magnitude in charge injection over the equivalent basic cell, when an unsaturated regulated cascode is used. Since the error currents are being stored by the basic cells in one phase and cancelled in another, the cell current will vary slightly giving rise to a small g_m change and hence to a small residual error. When an unsaturated regulated cascode is used the g_ms remain constant and this source of secondary error is eliminated.

In the above comparison, we have not attempted to compare the performance of the proposed algorithmic cell with the charge injection minimisation schemes currently available.[7,9] This is because the proposed cell, envisaged as a direct replacement for the basic cell, offers improved charge injection performance. Charge injection minimisation schemes may still be applied to yield even better performance.

The above improvement in charge injection performance has been achieved at the cost of increased area and power consumption. In typical system applications much of the chip area will be occupied by digital logic and consequently the price paid is not prohibitive.

Using the same basic cell, the proposed cell operates at one sixth the speed of the basic cell, because of the use of more complex clocking than before. Thus the proposed cell offers a significant improvement in the accuracy, with only a slight loss in speed. To assess the speed/accuracy trade-off of the new cell, its settling time was simulated, with a $10\,\mu A$ input current to 0.01%, using an unsaturated regulated cascode memory cell. The settling time for the cell was found to be 123 ns, giving a maximum operating frequency of 650 KHz for the new cell and 3.9 MHz for the basic cell. In this instance using the new cell has improved the charge injection by a factor of 46, thus giving a significant speed/accuracy improvement of 7.7 times.

Conclusions: A new high performance algorithmic switched-current memory cell has been proposed. This cell offers a significant improvement in the magnitude of charge injection and consequently the speed/accuracy ratio compared with that of the basic cell architecture. The accuracy of the cell is open to further improvement if additional cancellation techniques are applied or if high frequency performance is sacrificed.

The new cell is envisaged as a direct replacement for the basic cell and as such will find wide application in filtering and data conversion applications.

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